UTILITY PATENT APPLICATION TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR 1.53(b))*	Attorney Docket No.	0057-2511-2YY
	First Inventor or Application Identifier	Shuuichi UENO, et al.
	Title	SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ■ Fee Transmittal Form (e.g. PTO/SB/17)
(Submit an original and a duplicate for fee processing)
2. ■ Specification — Total Pages **29**
3. ■ Drawing(s) *(35 U.S.C. 113)* — Total Sheets **23**
4. ■ Oath or Declaration — Total Pages **4**
   a. ■ Newly executed (original)
   b. ☐ Copy from a prior application *(37 C.F.R. §1.63(d))*
   (for continuation/divisional with box 15 completed)
      i. ☐ DELETION OF INVENTOR(S)
      Signed statement attached deleting inventor(s) named in the prior application, see *37 C.F.R. §1.63(d)(2) and 1.33(b).*
5. ☐ Incorporation By Reference *(usable if box 4B is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4B, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

ACCOMPANYING APPLICATION PARTS

6. ☐ Assignment Papers (cover sheet & document(s))
7. ☐ 37 C.F.R. §3.73(b) Statement *(when there is an assignee)* ☐ Power of Attorney
8. ☐ English Translation Document *(if applicable)*
9. ■ Information Disclosure Statement (IDS)/PTO-1449 ■ Copies of IDS Citations (1)
10. ☐ Preliminary Amendment
11. ■ White Advance Serial No. Postcard
12. ☐ Small Entity Statement(s) ☐ Statement filed in prior application. Status still proper and desired.
13. ■ Certified Copy of Priority Document(s) (1)
(if foreign priority is claimed)
14. ■ Other: Notice of Priority

15. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below:*
☐ Continuation ☐ Divisional ☐ Continuation-in-part (CIP) of prior application no.:
Prior application information: Examiner: Group Art Unit:

16. Amend the specification by inserting before the first line the sentence:
☐ This application is a ☐ Continuation ☐ Division ☐ Continuation-in-part (CIP)
of application Serial No. Filed on

☐ This application claims priority of provisional application Serial No. Filed

17. CORRESPONDENCE ADDRESS

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VIRGINIA 22202
(703) 413-3000
FACSIMILE: (703) 413-2220

Name:	Marvin J. Spivak	Registration No.:	24,913
Signature:	[signature]	Date:	9/14/99
Name:	C. Irvin McClelland ~~Registration Number 21,124~~	Registration No.:	

TITLE OF THE INVENTION

Semiconductor Device and Manufacturing Method Thereof

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a semiconductor device in which a well is divided into a plurality of parts by a trench, and a method of manufacturing the semiconductor device.

Description of the Background Art

Semiconductor devices are usually formed by using a p-type semiconductor substrate (e.g., silicon substrate). As shown in Fig. 29, a p-channel transistor pT (source drain regions RN are of n-type) may be formed on a p-type semiconductor substrate 900, whereas in forming an n-channel transistor nT (source drain regions RP are of p-type), it is necessary to form a local n-type layer NW. The layer NW is called "well."

Wells are generally classified as thermal diffusion well and retro-grade well. In forming a thermal diffusion well NW, impurity N is implanted into a shallow position in a semiconductor substrate 900 (see Fig. 30), and the structure of Fig. 30 is subjected to heat treatment at high temperature for a prolonged time, so that the impurity N is diffused into the semiconductor substrate 900 (see Fig. 31), resulting in the thermal diffusion well NW. A retro-grade well MW is formed by implanting impurity N into a deep position in a semiconductor substrate 900, as shown in Fig. 32.

Fig. 33 shows the impurity concentration profile on the line A-A of Fig. 32. Since the retro-grade well is formed by implanting the impurity N, the impurity concentration profile can be set arbitrarily. In Fig. 33 it is controlled such that the impurity concentration has a maximum at a deep position P1 in the semiconductor substrate 900, and the impurity concentration at a shallow position P2 in the substrate 900 is higher than that of the substrate 900 and sufficiently lower than that of the channel.

This offers the merit that the transistor nT in the well NW is protected against the influence of the potential outside of the well NW.

In recent years, the decreased size of a transistor nT has created the need for increasing the impurity concentration of the well NW in order to suppress punch through. In some elements, therefore, a well NW is intentionally distributed so as to reach the main surface of a semiconductor substrate 900 for adjustment of the impurity concentration of the well NW.

Adjustment of impurity concentration is required to not only an n-channel transistor nT but also a p-channel transistor pT in some cases. In this case, a p-type well PW is formed (see Fig. 34).

Further, if it is desired to arbitrarily set the substrate potential of the p-channel transistor pT (i.e., the potential of a back gate), the well PW is electrically isolated from other regions by an n-type bottom well BNW and a well NW, as shown in Fig. 35.

When a well NW and a well PW are in contact with each other (see Fig. 36), both wells can be electrically isolated by a depletion layer DR to be generated at the interface therebetween. This merit is to permit an easy electrical isolation between the well NW and the well PW. The depletion layer DR, however, has a tendency to extend and thus it might extend throughout a zone EUR. This causes the demerit that it is impossible to form a transistor in the zone EUR. An element isolation film Ta is formed in the zone EUR in which no transistor is formed (see Fig. 37).

To overcome the above demerit, a trench is formed at the boundary between the well NW and the well PW, and an element isolation film Tb is buried in the trench (see Fig. 38). Thereby, no depletion layer occurs at a well boundary between the well NW and the well PW (i.e., in the vicinity of the element isolation film Tb). This offers the merit that a transistor can be formed in the zone EUR by reducing the margin from the

well boundary to a transistor. Unfortunately, the step of employing a trench is complicated and expensive which are the drawbacks of this step.

Two methods of well isolation using a trench are presently proposed. One comprises a first step of forming an element isolation film and a second step of forming n-type and p-type wells. Fig. 39 shows a structure formed by this method. With this method, no disadvantages are caused by reducing the margin from a well boundary to an element, however, the well isolation process using a trench involves the above two steps. Accordingly, this method is time-consuming and increases the manufacturing cost.

The other is to conduct the above first and second steps at the same time. Fig. 40 shows a structure formed by this method. The structure of Fig. 40 is realized by forming a deep element isolation film Tb such as to correspond to the depth of wells NW and PW (see Fig. 41), or forming shallow wells NW and PW such as to correspond to the thickness of an element isolation film Tb (see Fig. 42), alternatively, in a combination of these. In any event, the depth of the element isolation films Tb is evened and each of the wells NW and PW is divided into a plurality of parts by the element isolation film Tb.

It is, however, necessary to open a contact 201 per active region, namely, per well (see Fig. 43), in order to apply the desired potential to each of the isolated wells NW and PW. Thus it is necessary to increase the area of a well by the amount of a region CR for providing the contact 201. That is, as a whole, it fails to take full advantage of the merit in terms of area that is obtained by the trench as stated earlier with respect to Fig. 38. Also, there is a problem that layout area is increased by the amount of the region CR to be provided per well.

Accordingly, an object of the present invention is to provide a semiconductor device in which a well is divided into a plurality of parts by a trench, to effect a reduction in layout area, as well as a method of manufacturing the semiconductor device.

SUMMARY OF THE INVENTION

According to a first aspect of the present invention, a semiconductor device comprises: a semiconductor substrate; an element isolation film formed such as to have to a predetermined depth from a main surface of the semiconductor substrate, the element isolation film dividing the area from the main surface to the depth into a plurality of first regions; first wells formed in the first regions, respectively; and a second well formed in a second region deeper than the first wells in the semiconductor substrate, the second well being in contact with some of the first wells.

According to a second aspect, the semiconductor device according to the first aspect is characterized in that the first and second wells of the first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and the first and second wells on the other side are of a second conductivity type.

According to a third aspect, the semiconductor device according to the second aspect is characterized in that the second well of the first conductivity type and the second well of the second conductivity type are not in contact with each other.

According to a fourth aspect, the semiconductor device according to the first aspect is characterized in that the second well is formed on only one side of the second region with reference to a predetermined boundary.

According to a fifth aspect, the semiconductor device according to the fourth aspect is characterized in that the second well is formed in a memory cell part in the second region.

According to a sixth aspect, the semiconductor device according to the first aspect is characterized in that the second well is formed only in the vicinity of the bottom of the element isolation film in the second region.

According to a seventh aspect, the semiconductor device according to the first

aspect is characterized in that each impurity concentration of the first and second wells is higher as being closer to a boundary part between the first and second regions.

According to an eighth aspect, the semiconductor device according to the first aspect further comprises a third well formed in a third region deeper than the second region in the semiconductor substrate.

According to a ninth aspect, a method of manufacturing a semiconductor device comprises the steps of: (a) forming an element isolation film such as to have a predetermined depth from a main surface of a semiconductor substrate, to divide the area from the main surface to the depth into a plurality of first regions; and (b) forming first wells in the first regions, respectively, and forming a second well making contact with some of the first wells, in a second region deeper than the first wells in the semiconductor substrate.

According to a tenth aspect, the method according to the ninth aspect is characterized in that the step (b) comprises the steps of (b-1) covering, with a first resist, one side region of the main surface with reference to a predetermined boundary in the semiconductor substrate; (b-2) implanting impurity of a first conductivity type into the first region by using the first resist as a mask; (b-3) implanting impurity of the first conductivity type into the second region by using the first resist as a mask; (b-4) removing the first resist; (b-5) covering, with a second resist, the other side region of the main surface with reference to the boundary in the semiconductor substrate; (b-6) implanting impurity of a second conductivity type into the first region by using the second resist as a mask; (b-7) implanting impurity of the second conductivity type into the second region by using the second resist as a mask; and (b-8) removing the second resist.

According to an eleventh aspect, the method according to the ninth aspect is characterized in that the step (b) comprises the steps of: (b-1) covering, with a first resist,

one side region of the main surface with reference to a predetermined boundary in the semiconductor substrate; (b-2) implanting impurity of a first conductivity type into the first region by using the first resist as a mask; (b-3) reforming the first resist such as to be thicker, as a second resist; (b-4) implanting impurity of the first conductivity type into the second region by using the second resist as a mask; (b-5) removing the second resist; (b-6) covering, with a third resist, the other side region of the main surface with reference to the boundary in the semiconductor substrate; (b-7) implanting impurity of a second conductivity type into the first region by using the third resist as a mask; (b-8) reforming the third resist such as to be thicker, as a fourth resist; (b-9) implanting impurity of the second conductivity type into the second region by using the fourth resist as a mask; and (b-10) removing the fourth resist.

According to a twelfth aspect, a method of manufacturing a semiconductor device comprises the steps of: (a) forming a trench such as to have a predetermined depth from a main surface of a semiconductor substrate, to divide the area from the main surface to the depth into a plurality of regions in the semiconductor substrate; (b) implanting a first impurity from above the main surface into the trench; and (c) implanting a second impurity from above the main surface into the regions.

The first aspect enables that some of the first wells are electrically connected one another through the second well. It is therefore possible to apply a potential to all the first wells by placing a contact in at least one of the first wells. This leads to a reduction in layout area.

The second aspect allows the electrical connection between the first and second wells to be performed each conductivity type separately.

The third aspect has no chance that a depletion layer extends from the third region in the second region to the first well because the second well of the first

conductivity type and the second well of the second conductivity type are not in contact with each other.

The fourth aspect enables to simplify the process and reduce the manufacturing cost, as compared with a semiconductor device of the second aspect.

The fifth aspect is extremely effective when applied to the memory cell part alone, in terms of simplification in process, manufacturing cost reduction and layout area reduction.

The sixth aspect enables to form the second well by utilizing a trench, for example.

The seventh aspect enables to prevent a depletion layer from extending to the first well even if the depletion layer occurs in the second well, by setting the impurity concentration of the first and second wells at the boundary between the first and second regions, to a sufficiently large value.

The eighth aspect allows the potential of the first and second wells to be set independently of the potential at a position lower than the third well.

The ninth aspect enables to manufacture a semiconductor device of the first aspect, and simplify the step of providing a contact and the step of providing wiring connected to the contact because the contact may be provided at least one of the first wells.

The tenth aspect enables to manufacture a semiconductor device of the second aspect, and simplify the manufacturing steps because a single resist is used in impurity implantation into both first and second regions.

The eleventh aspect enables to manufacture a semiconductor device of the third aspect, and easily obtain the structure in which the second well of the first conductivity type and the second well of the second conductivity type are not in contact with each

other, by utilizing the feature that the taper of a resist becomes significant when the resist is thickened. In addition, even if impurity lift phenomenon occurs due to a marked taper of the second and fourth resists, the impurity related to the lift phenomenon is to be contained in the first well, thereby suppressing a noticeable change in impurity concentration profile.

The twelfth aspect enables to manufacture a semiconductor device of the sixth aspect, and form the second well by utilizing a trench.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view showing schematically the structure of a semiconductor device according to a first preferred embodiment of the present invention;

Fig. 2 is a cross-sectional view illustrating the structure of the semiconductor device of the first preferred embodiment;

Fig. 3 is a graph showing the impurity concentration of the well in the semiconductor device of the first preferred embodiment;

Figs. 4 to 9 are cross-sectional views showing a sequence of steps in a method of manufacturing a semiconductor device according to a second preferred embodiment;

Fig. 10 is a cross-sectional view illustrating the structure of a semiconductor device according to a third preferred embodiment;

Figs. 11 to 14 are cross-sectional views illustrating a sequence of steps in a method of manufacturing a semiconductor device according to a fourth preferred embodiment;

Fig. 15 is a cross-sectional view illustrating the structure of a semiconductor

device according to a fifth preferred embodiment;

Figs. 16 to 21 are cross-sectional views showing a sequence of steps in a method of manufacturing a semiconductor device according to a sixth preferred embodiment;

Fig. 22 is a cross-sectional view illustrating the structure of a semiconductor device according to a seventh preferred embodiment;

Fig. 23 is a cross-sectional view illustrating the structure of a semiconductor device according to an eighth preferred embodiment;

Fig. 24 is a cross-sectional view illustrating the structure of a semiconductor device according to a ninth preferred embodiment;

Figs. 25 and 26 are plan views illustrating the structure of a semiconductor device of the ninth preferred embodiment;

Fig. 27 is a cross-sectional view illustrating the structure of a semiconductor device according to a tenth preferred embodiment;

Fig. 28 is a cross-sectional view illustrating the structure of a semiconductor device according to an eleventh preferred embodiment;

Figs. 29 to 32 are cross-sectional views illustrating the structure of a conventional semiconductor device;

Fig. 33 is a graph showing the impurity concentration of a well in a conventional semiconductor device; and

Figs. 34 to 45 are cross-sectional views illustrating the structure of a conventional semiconductor device.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Preferred Embodiment

Fig. 1 is a plan view showing schematically the structure of a semiconductor

device according to a first preferred embodiment of the present invention. Fig. 2 is a cross-sectional view along the line II-II of Fig. 1.

Referring to Figs. 1 and 2, an element isolation film T which is for example an insulating film of SiO_2 is formed such as to have depth L1 from the main surface of a p-type silicon semiconductor substrate 100. The element isolation film T divides the area from the main surface of the semiconductor substrate 100 to the depth L1 in the substrate 100 into a plurality of first regions R1. The depth L1 is from 1,000 angstrom to 10,000 angstrom.

A first well W1 is formed in each of the first regions R1. In the semiconductor substrate 100, a second well W2 is formed in a second region R2 deeper than the first well W1. The second well W2 is in contact with some of the first wells W1.

In accordance with the first preferred embodiment, distance LW1 from the main surface of the semiconductor substrate 100 to the bottom face of the first well W1 is longer than the depth L1 from the main surface of the semiconductor substrate 100 to the bottom face of the element isolation film T. The distance LW1 is for example 1.1 times the depth L1. Thickness LW2 of the second well W2 is smaller than the depth L1. The thickness LW2 is for example 0.9 times the depth L1.

In the second region R2 and the first regions R1, the first well W1 and the second well W2 on one side region Ra with reference to a predetermined boundary BL passing through the top and bottom of the element isolation film T are of n-type, and the first well W1 and the second well W2 on the other side region Rb are of p-type.

Fig. 3 shows the impurity concentration on the line B-B of Fig. 2. As shown in Fig. 3, both impurity concentration of the first well W1 and the second well W2 increase as they approach a boundary part BW between the first region R1 and the second

region R2 (which part is located in the region consisting of the first and second regions R1 and R2, including the boundary between the regions R1 and R2). The impurity concentration of the first well W1 has a maximum in the vicinity of the bottom face of the element isolation film T (i.e., the trench bottom face), and its value is, for example, $1\times 10^{18}/cm^3$. The impurity concentration of the second well W2 also has a maximum in the vicinity of the trench bottom face, and its value is, for example, $5\times 10^{18}/cm^3$.

A single element (e.g., an MOS transistor) is formed in a single first region R1. When an MOS transistor is formed in the first region R1, the first well W1 functions to determine the impurity concentration between source and drain.

A comparison of the first preferred embodiment with prior art is made as below. In the structure of Fig. 36, the impurity concentration of the n-type well NW and the p-type well PW is set appropriately such that the depletion layer DR extends suitably, thereby isolating the n-type first well W1 and the p-type first well W1 with each other. Whereas in the structure of Fig. 2, the n-type first well W1 and the p-type first well W1 can be isolated by the element isolation film T provided therebetween, instead of a depletion layer. Therefore, the impurity concentration of the n-type first well W1 and the p-type first well W1 can be set more optionally than that in the structure of Fig. 36.

Further, the structure of Fig. 2 is free from such a well boundary as in the structure of Fig. 36, and no depletion layer is present in the vicinity of a region 3 in Fig. 2, thus causing no disadvantages in reducing the margin from the region R3 to the MOS transistor.

Since in the structure of Fig. 2, the n-type second well W2 and the p-type second well W2 are in contact with each other at the boundary BL in the second region R2, a depletion layer extends from such an interface. By this depletion layer, the n-type second well W2 and the p-type second well W2 are isolated with each other. It is

possible to prevent the depletion layer from extending from the interface between the n-type second well W2 and the p-type second well W2 to the first well W1, by setting such that the impurity concentration of the first and second wells W1 and W2 is sufficiently high in the vicinity of the trench bottom face of the element isolation film T (see Fig. 3).

The structure of Fig. 43 requires a region CR for making contact with the first well W1 per the first well W1, in order to apply a potential to all the first wells W1. Whereas in the structure of Fig. 2, the second well W2 makes contact with some of the first wells W1 to establish electrical contact therewith. It is therefore possible to apply a potential to all the first wells W1 by placing a contact in at least one of the first wells W1. It is also possible to reduce layout area by the amount of the reduced contacts 201.

In addition, the electrical connection between the first well W1 and the second well W2 can be performed per n-type and p-type individually.

Second Preferred Embodiment

A method of manufacturing a semiconductor device with the structure as stated in the first preferred embodiment will be described by referring to Figs. 4 to 9.

Firstly, a trench is formed at depth L1 (i.e., 1,000-10,000 angstrom) from the main surface of a p-type semiconductor substrate by for example etching, and an element isolation film T is formed in the trench. By the element isolation film T, the area from the main surface of the semiconductor substrate 100 to the depth L1 in the substrate 100 is divided into a plurality of first regions R1 (see Fig. 4).

Region Rb in the main surface of the semiconductor substrate 100 is covered with a resist MP1. By using the resist MP1 as a mask, an n-type impurity N1 is implanted from above a region Ra in the main surface of the semiconductor substrate 100 to the first regions R1, thereby forming an n-type first well W1 in the first region R1 (see Fig. 5).

For example, boron is used as the impurity N1, and its dose is $1\times10^{13}/cm^2$. Distance LW1 from the main surface of the semiconductor substrate 100 to the bottom face of the first well W1 may be smaller than the depth L1 from the main surface of the substrate 100 to the bottom face of the element isolation film T, and the distance LW1 is 0.9 times the depth L1, for example.

Then, by using the resist MP1 as a mask, an n-type impurity N2 is implanted from above the region Ra of the semiconductor substrate 100 to the second region R2, thereby forming an n-type second well W2 in the second region R2 (see Fig. 6).

For example, boron is used as the impurity N2, and its dose is $1\times10^{13}/cm^2$. Thickness LW2 of the second well W2 may be longer than the depth L1, and it is 1.1 times the depth L1, for example.

After the resist MP1 is removed, the region Ra in the main surface of the semiconductor substrate 100 is covered with a resist MN1. By using the resist MN1 as a mask, a p-type impurity P1 is implanted from above the region Rb in the main surface of the substrate 100 to the first region R1, thereby forming a p-type first well W1 in the first region R1 (see Fig. 7).

For example, phosphorus is used as the impurity P1, and its dose is $1\times10^{13}/cm^2$. Distance LW1 from the main surface of the semiconductor substrate 100 to the bottom face of the first well W1 may be smaller than the depth L1 from the main surface of the substrate 100 to the bottom face of the element isolation film T, and the distance LW1 is 0.9 times the depth L1, for example.

Then, by using the resist MN1 as a mask, a p-type impurity P2 is implanted from above the region Rb of the semiconductor substrate 100 to the second region R2, thereby forming a p-type second well W2 in the second region R2 (see Fig. 8).

For example, phosphorus is used as the impurity P2, and its dose is $1\times$

$10^{13}/cm^2$. Thickness LW2 of the second well W2 may be larger than the depth L1 and it is for example 1.1 times the depth L1.

The resist MN1 is then removed to obtain the structure as described in the first preferred embodiment (see Fig. 9). Thus, the first well W1 is formed per first region R1, and the second well W2 having contact with some of the first wells W1 is formed in the second region R2 deeper than the first well W1 in the semiconductor substrate 100 (see Figs. 5 to 9).

Thereafter, a gate oxide film (not shown) having for example a thickness of 50 angstrom is formed and an element such as a transistor (not shown) is formed in the first region R1 by for example channel doping. This is followed by predetermined various processes (e.g., assembler process), resulting in a semiconductor device.

As stated in the first preferred embodiment, since a contact is provided at least one of the first wells W1, it is possible to simplify the step of providing contacts and the step of providing wiring connected to the contacts.

In addition, the resist MP1 is used in implanting both impurities N1 and N2, and the resist MN1 is used in implanting both impurities P1 and P2, thus simplifying the manufacturing steps.

Third Preferred Embodiment

Fig. 10 is a cross-sectional view illustrating the structure of a semiconductor device according to a third preferred embodiment. This embodiment is a modification of the first preferred embodiment. In the first preferred embodiment the n-type second well W2 and the p-type second well W2 are in contact with each other at the boundary BL, as shown in Fig. 2. On the other hand, in the third preferred embodiment the n-type and p-type second wells W2 are not in contact with each other at a boundary BL, as shown in Fig. 10.

A first well W1 and a second well W2 on the sides of an element isolation film T at the boundary BL are in contact with each other. For example, a 1 μm contact length L2 between the first and second wells W1 and W2 is sufficient.

Since in the structure of Fig. 10, the n-type second well W2 and the p-type second well W2 are not in contact with each other, there is no possibility that a depletion layer extends from the boundary BL in the second region R2 to the first well W1.

Fourth Preferred Embodiment

A method of manufacturing a semiconductor device with the structure as described in the third preferred embodiment will be described by referring to Figs. 4 and 11 to 14.

Firstly, a trench is formed at depth L1 (i.e., 1,000-10,000 angstrom) from the main surface of a p-type semiconductor substrate by for example etching, and an element isolation film T is formed in the trench. By the element isolation film T, the area from the main surface of the semiconductor substrate 100 to the depth L1 in the substrate 100 is divided into a plurality of first regions R1 (see Fig. 4).

Region Rb in the main surface of the semiconductor substrate 100 is covered with a resist MP1. By using the resist MP1 as a mask, an n-type impurity N1 is implanted from above a region Ra in the main surface of the semiconductor substrate 100 to the first regions R1, thereby forming an n-type first well W1 in the first region R1 (see Fig. 11).

For example, boron is used as the impurity N1, and its dose is $1\times10^{13}/cm^2$. Distance LW1 is 0.9 times the depth L1, for example.

Then, the resist MP1 is reformed such as to be thicker, as a resist MP2 (see Fig. 12). Specifically, for example, the resist MP1 is removed and the region Rb in the semiconductor substrate 100 is covered with a resist MP2 in the same conditions as stated

earlier. Here, it is set such that the resist MP2 is thicker than the resist MP1. Alternatively, the resist MP1 may be left and then reformed as a resist MP2 having a greater thickness by stacking a resist on the resist MP1.

This is because that the resist MP2 is required to have a greater thickness in order to prevent the impurity N2 from passing through the resist MP2 and being implanted into an undesirable region since the impurity N2 implanted later is implanted at an energy higher than that in the impurity N1. As shown in Fig. 12, taper is more noticeable as the resist MP2 becomes thicker, and the taper part of the resist MP2 extends to the region Ra beyond the boundary BL.

Then, by using the resist MP2 as a mask, an n-type impurity N2 is implanted from above the region Ra of the semiconductor substrate 100 to the second region R2, thereby forming an n-type second well W2 in the second region R2.

For example, boron is used as the impurity N2, and its dose is $1\times10^{13}/cm^2$. Thickness LW2 is 1.1 times the depth L1, for example.

After the resist MP2 is removed, the region Ra in the main surface of the semiconductor substrate 100 is covered with a resist MN1. By using the resist MN1 as a mask, a p-type impurity P1 is implanted from above the region Rb of the main surface in the substrate 100 to the first region R1, thereby forming a p-type first well W1 in the first region R1 (see Fig. 13).

For example, phosphorus is used as the impurity P1, and its dose is $1\times10^{13}/cm^2$. Distance LW1 is 0.9 times the depth L1, for example.

Then, the resist MN1 is reformed such as to be thicker, as a resist MP2 (see Fig. 14). Specifically, for example, the resist MN1 is removed and the region Ra in the semiconductor substrate 100 is covered with a resist MN2 in the same conditions as stated earlier. Here, it is set such that the resist MN2 is thicker than the resist MN1.

Alternatively, the resist MN1 may be left and then reformed as a resist MN2 having a great thickness by stacking a resist on the resist MN1.

This is because that the resist MN2 is required to have a great thickness in order to prevent the impurity P2 from passing through the resist MN2 and being implanted into an undesirable region since the impurity P2 implanted later is implanted at an energy higher than that in the impurity P1. As the resist MN2 becomes thicker, taper is more noticeable and, as shown in Fig. 14, the taper part of the resist MN2 extends to the region Rb beyond the boundary BL.

Then, by using the resist MN2 as a mask, a p-type impurity P2 is implanted from above the region Rb in the main surface of the semiconductor substrate 100 to the second region R2, thereby forming a p-type second well W2 in the second region R2.

For example, phosphorus is used as the impurity P2, and its dose is $1\times 10^{13}/cm^2$. Thickness LW2 is 1.1 times the depth L1, for example.

The resist MN2 is then removed to obtain the structure as described in the third preferred embodiment. Thus, the first well W1 is formed in each of the first regions R1, and the second well W2 having contact with some of the first wells W1 is formed in the second region R2 deeper than the first wells W1 in the semiconductor substrate 100 (see Figs. 11 to 14).

Thereafter, a gate oxide film (not shown) with a thickness of 50 angstrom, for example, an element such as a transistor (not shown) is formed in the first region R1 by channel doping, for example. This is followed by predetermined various processes (e.g., assembler process), resulting in a semiconductor device.

Effects of the fourth preferred embodiment will be described. The structure in which the n-type second well W2 and the p-type second well W2 are not in contact with each other is obtained easily by utilizing the feature that the taper of the resists MP2 and

MN2 becomes significant when the resists MP2 and MN2 is thickened.

It is, however, known that the following drawbacks occur when taper becomes significant. A comparison is made between the case where a well W is formed by implanting an impurity D1 into a second region R2 in a semiconductor substrate 900 by using, as a mask, a resist M1 whose taper is insignificant (see Fig. 44), and the case where a well W is formed by implanting an impurity D1 into a second region R2 in a semiconductor substrate 900 by using, as a mask, a resist M2 whose taper is significant (see Fig. 45). In the structure of Fig. 45, the impurity D1 passes through the taper of the resist M2, so that the impurity D1 is implanted into a region WR immediately beneath the taper, from a deep position to a shallow position in the semiconductor substrate 900 (this is called as lift phenomenon). On the other hand, such impurity lift phenomenon does not occur in the structure of Fig. 44. The impurity lift phenomenon may change the impurity concentration profile. In particular, the difference in polarity between the semiconductor substrate 900 and the impurity D1 would cause a great difference in electrical properties.

As shown in Figs. 12 and 14, the first well W1 is already formed in the first region before the impurities N2 and P2 are implanted into the second region R2 of the semiconductor substrate 100. Therefore, even if the impurity lift phenomenon occurs, the impurity related to the lift phenomenon is to be contained in the first well W1, thereby making it possible to suppress a marked change in the impurity concentration profile.

Fifth Preferred Embodiment

Fig. 15 is a cross-sectional view illustrating the structure of a semiconductor device according to a fifth preferred embodiment. This embodiment is a modification of the third preferred embodiment. As shown in Fig. 10, in the third preferred embodiment the second well W2 is formed throughout the region beneath the first regions R1 (except

for the first regions R1 on both sides of the boundary BL). Whereas in the fifth preferred embodiment the second well W2 is formed only in the vicinity of the bottom of a second region R2 of an element isolation film T, along the bottom of the second region R2 of the film T, as shown in Fig. 15. With this structure, the second well W2 makes contact with some of the first wells W1, thus establishing electrical contact therewith.

Sixth Preferred Embodiment

A method of manufacturing a semiconductor device with the structure as stated in the fifth preferred embodiment will be described by referring to Figs. 16 to 21.

Firstly, in a flat main surface of a p-type semiconductor substrate 100 prior to forming a trench (groove), the area except for a region whereat a trench will be formed is covered with a resist MT. By using the resist MT as a mask, the semiconductor substrate 100 is subjected to etching for forming a trench T1 (groove) with depth L1 (1,000-100,000 angstrom) from the main surface of the substrate 100. By the trench T1, the area from the main surface of the semiconductor substrate 100 to the depth L1 in the substrate 100 is divided into a plurality of first regions R1 (see Fig. 16).

Then, the trench T1 at a boundary BL and a region Rb in the main surface of the semiconductor substrate 100 are covered with a resist MP2. By using the resist MP2 and the resist MT as masks, an n-type impurity N2 is implanted from above the region Ra of the main surface in the substrate 100 to the trench T1. This enables to form an n-type well W2 on the inner walls of the trench T1 and beneath the element isolation film T of the second region R2 (see Fig. 17).

For example, boron is used as the impurity N2, and its dose is $1\times10^{13}/cm^2$. Thickness LW2 is 0.1 times the depth L1, for example.

After the resist MP2 is removed (the resist MT is left), the trench T1 at the boundary BL and the region Ra of the main surface in the semiconductor substrate 100

are covered with a resist MN2. By using the resist MN2 and the resist MT as masks, a p-type impurity P2 is implanted from above the region Rb of the main surface in the substrate 100 to the trench T1. Thereby, a p-type second well W2 is formed on the inner walls of the trench T1 and beneath the element isolation film T (see Fig. 18).

For example, phosphorus is used as the impurity P2, and its dopand dose is 1×10^{13}/cm. Distance LW2 is 0.1 times the depth L1, for example.

After the resist MN2 and the resist MT are removed, an element isolation film T is formed in the trench T1 (see Fig. 19). If necessary, the element isolation film T is flattened.

The region Rb in the main surface of the semiconductor substrate 100 is covered with a resist MP1. Then, by using the resist MP1 as a mask, an n-type impurity N1 is implanted from above the region Ra of the main surface in the semiconductor substrate 100 to the first region R1, thereby forming an n-type first well W1 in the first region R1 (see Fig. 20).

For example, boron is used as the impurity N1, and its dopand dose is 1×10^{13}/cm. Distance LW1 is 0.9 times the depth L1, for example.

After the resist MP1 is removed, the region Ra in the main surface of the semiconductor substrate 100 is covered with a resist MN1. By using the resist MN1 as a mask, a p-type impurity P1 is implanted from above the region Rb of the main surface in the substrate 100 to the first region R1, thereby forming a p-type first well W1 in the first region R1 (see Fig. 21).

For example, phosphorus is used as the impurity P1, and its dopand dose is 1×10^{13}/cm. Distance LW1 is 0.9 times the depth L1, for example.

The resist MN1 is then removed to obtain the structure as described in the fifth preferred embodiment.

Thereafter, a gate oxide film (not shown) with a thickness of 50 angstrom, for example, is formed and an element such as a transistor (not shown) is formed in the first region R1 by channel doping, for example. This is followed by predetermined various processes (e.g., assembler process), resulting in a semiconductor device.

As described above, the second well W2 can be formed by utilizing the trench T1 and the resist MT used in forming the trench T1.

Seventh Preferred Embodiment

Fig. 22 is a cross-sectional view illustrating the structure of a semiconductor device according to a seventh preferred embodiment. This embodiment is a modification of the first to sixth preferred embodiments. In the first to sixth preferred embodiments, the n-type second well W2 and the p-type second well W2 are both formed. Whereas in the seventh preferred embodiment, for a p-type semiconductor substrate 100, a p-type second well W2 is omitted and only an n-type second well W2 is formed. For an n-type semiconductor substrate 100, an n-type second well W2 is omitted and only a p-type second well W2 is formed.

Fig. 22 shows the case where a p-type second well W2 is eliminated from the structure of Fig. 9.

Thus, the second well W2 is formed on only one side of the second region R2 with reference to the boundary BL.

It is possible to simplify the process and reduce the manufacturing cost by the omission of either the p-type second well W2 or the n-type second well W2. For instance, the step of implanting the impurity P2 as shown in Fig. 8 can be omitted in the second preferred embodiment, and the step of forming the resist MN2 and the step of implanting the impurity P2 as shown in Figs. 14 and 18 can be omitted in the fourth and sixth preferred embodiments, respectively.

Eighth Preferred Embodiment

Fig. 23 is a cross-sectional view illustrating the structure of a semiconductor device according to an eighth preferred embodiment. This embodiment is a modification of the first to sixth preferred embodiments. In the first to sixth preferred embodiments, the n-type second well W2 and the p-type second well W2 are both formed. Whereas in the eighth preferred embodiment, an unnecessary n-type second well W2 or p-type second well W2 is omitted as needed.

Fig. 23 shows the case where the n-type second well W2 is eliminated from the structure of Fig. 9. In Fig. 23, an element isolation film T and a first region R1 are covered with an insulating film 300, and a plurality of n-type first wells W1 are electrically connected one another by a contact 201 and a wiring 202. Therefore, even if the n-type second well W2 is omitted, it is possible to apply a potential to each of the n-type first wells W1.

Thus, the second well W2 is formed on only one side of the second region R2 with reference to the boundary BL.

It is possible to simplify the process and reduce the manufacturing cost by the omission of either the p-type second well W2 or the n-type second well W2. For instance, the step of implanting the impurity N2 as shown in Fig. 6 can be omitted in the second preferred embodiment, and the step of forming the resist MP2 and the step of implanting the impurity N2 as shown in Figs. 12 and 17 can be omitted in the fourth and sixth preferred embodiments, respectively.

Ninth Preferred Embodiment

A ninth preferred embodiment relates to the foregoing embodiments 1 to 8. There is no need to provide a second well W2 for each of elements to be formed in a semiconductor substrate 100, and the second well W2 may be formed for an element

which necessitates the formation of the second well W2. It is possible to simplify the process and reduce the manufacturing cost by selecting an element for providing a second well W2.

When a semiconductor device is a SRAM, a second well W2 may be provided in a memory cell part SR, as shown in Fig. 24. The references used for Fig. 23 are used again Fig. 24.

As been well known, a memory cell is the minimum unit of memory storage, and it is a region for storing one bit, for example. The term "memory cell region" is understood to mean a region in which a memory cell is provided.

Fig. 25 shows one example of plan views of a single memory cell in an SRAM. The references used for Fig. 24 are used again Fig. 25. Fig. 26 shows the structure that is obtained by eliminating a wiring 202 and an element isolation film T from the structure of Fig. 25. In an SRAM, there are formed, for example, several millions of the unit of the structure of Fig. 26. It is therefore extremely effective to select the memory cell part SR for providing the second well W2. That is, the second well W2 is provided only for the memory cell part SR in a plurality of elements in the SRAM, and the second wells W2 is omitted for other elements, thus simplifying the process and reducing the manufacturing cost. In addition, there is no need to provide a contact 201 for each of, for example, several millions memory cells, leading to an extremely small layout area.

Tenth Preferred Embodiment

Fig. 27 is a cross-sectional view illustrating the structure of a semiconductor device according to a tenth preferred embodiment. Fig. 24 shows the case where the second well W2 is provided in the memory cell part SR of the SRAM. In addition to this, a second well W2 may be provided in a memory cell part DR of a DRAM in this embodiment.

Eleventh Preferred Embodiment

Fig. 28 is a cross-sectional view illustrating the structure of a semiconductor device according to an eleventh preferred embodiment. This embodiment is a modification of the foregoing embodiments 1 to 10. In the tenth preferred embodiment, a third well W3 is further provided in a third region R3 deeper than a second region R2 in a semiconductor substrate 100.

Fig. 28 indicates the case where an n-type third well W3 is added to the structure of Fig. 9, for example. Thereby, first and second wells W1 and W2 can be electrically isolated with each other from a region lower than the third well W3. This enables to individually set the potential of the first and second wells W1 and W2 from the potential at a position lower than the third well W3. It is also possible to utilize the third well W3 as a countermeasure for soft errors (i.e., the phenomenon that the storage contents of a memory is vanished).

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor substrate;

an element isolation film formed such as to have a predetermined depth from a main surface of said semiconductor substrate, said element isolation film dividing the area from said main surface to said depth into a plurality of first regions;

first wells formed in said first regions, respectively; and

a second well formed in a second region deeper than said first wells in said semiconductor substrate, said second well being in contact with some of said first wells.

2. A semiconductor device according to claim 1 wherein said first and second wells of said first and second regions on one side with reference to a predetermined boundary are of a first conductivity type, and said first and second wells on the other side are of a second conductivity type.

3. A semiconductor device according to claim 2 wherein said second well of said first conductivity type and said second well of said second conductivity type are not in contact with each other.

4. A semiconductor device according to claim 1 wherein said second well is formed on only one side of said second region with reference to a predetermined boundary.

5. A semiconductor device according to claim 4 wherein said second well is formed in a memory cell part in said second region.

6. A semiconductor device according to claim 1 wherein said second well is formed only in the vicinity of the bottom of said element isolation film in said second region.

7. A semiconductor device according to claim 1 wherein each impurity concentration of said first and second wells is higher as being closer to a boundary part between said first and second regions.

8. A semiconductor device according to claim 1 further comprising a third well formed in a third region deeper than said second region in said semiconductor substrate.

9. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming an element isolation film such as to have a predetermined depth from a main surface of a semiconductor substrate, to divide the area from said main surface to said depth into a plurality of first regions; and

(b) forming first wells in said first regions, respectively, and forming a second well making contact with some of said first wells, in a second region deeper than said first wells in said semiconductor substrate.

10. A method according to claim 9 wherein said step (b) comprising the steps of:

(b-1) covering, with a first resist, one side region of said main surface with

reference to a predetermined boundary in said semiconductor substrate;

(b-2) implanting impurity of a first conductivity type into said first region by using said first resist as a mask;

(b-3) implanting impurity of the first conductivity type into said second region by using said first resist as a mask;

(b-4) removing said first resist;

(b-5) covering, with a second resist, the other side region of said main surface with reference to said boundary in said semiconductor substrate;

(b-6) implanting impurity of a second conductivity type into said first region by using said second resist as a mask;

(b-7) implanting impurity of the second conductivity type into said second region by using said second resist as a mask; and

(b-8) removing said second resist.

11. A method according to claim 9 wherein said step (b) comprising the steps of:

(b-1) covering, with a first resist, one side region of said main surface with reference to a predetermined boundary in said semiconductor substrate;

(b-2) implanting impurity of a first conductivity type into said first region by using said first resist as a mask;

(b-3) reforming said first resist such as to be thicker, as a second resist;

(b-4) implanting impurity of the first conductivity type into said second region by using said second resist as a mask;

(b-5) removing said second resist;

(b-6) covering, with a third resist, the other side region of said main surface

with reference to said boundary in said semiconductor substrate;

(b-7) implanting impurity of a second conductivity type into said first region by using said third resist as a mask;

(b-8) reforming said third resist such as to be thicker, as a fourth resist;

(b-9) implanting impurity of the second conductivity type into said second region by using said fourth resist as a mask; and

(b-10) removing said fourth resist.

12. A method of manufacturing a semiconductor device comprising the steps of:

(a) forming a trench such as to have a predetermined depth from a main surface of a semiconductor substrate, to divide the area from said main surface to said depth into a plurality of regions in said semiconductor substrate;

(b) implanting a first impurity from above said main surface into said trench; and

(c) implanting a second impurity from above said main surface into said regions.

ABSTRACT OF THE DISCLOSURE

Provided are a semiconductor device in which a well is divided into a plurality of parts by a trench, to effect a reduction in layout area, and a manufacturing method thereof. In the semiconductor device, an element isolation film (T) is formed such as to have to a depth (L1) from the main surface of a semiconductor substrate (100), and the area from the main surface of the substrate (100) to the depth (L1) is divided into a plurality of first regions (R1). A first well (W1) is formed in each of the first regions (R1). A second well (W2) is formed in a second region (R2) deeper than the first well (W1) in the substrate (100), and the second well (W2) is in contact with some of the first wells (W1).

FIG. 1

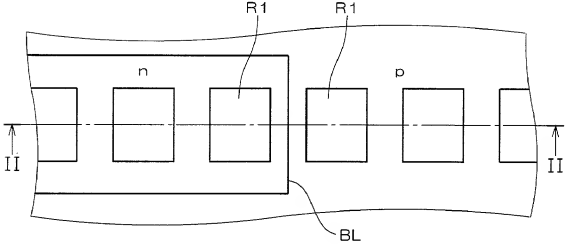

R1
R1
n
p
II
II
BL

FIG. 2

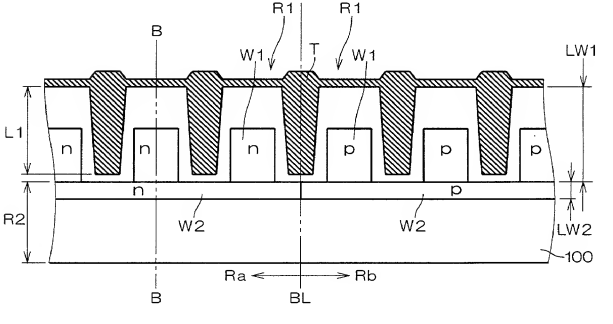

R1
R1
B
W1
T
W1
LW1
L1
n
n
n
p
p
p
n
p
R2
W2
W2
LW2
100
Ra
Rb
B
BL

FIG. 3

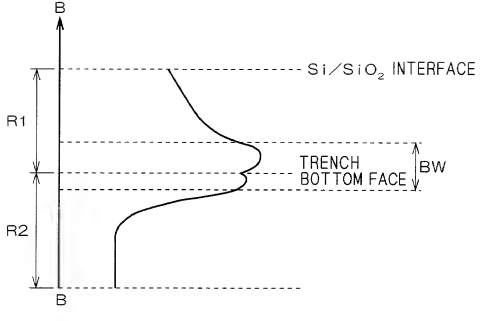

B
Si/SiO2 INTERFACE
R1
TRENCH
BOTTOM FACE
BW
R2
B

FIG. 4

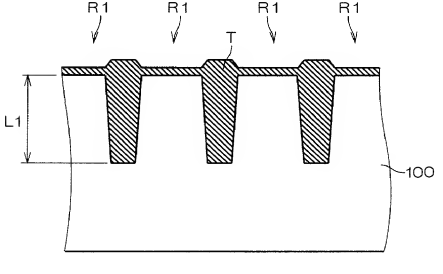

R1
R1
R1
R1
T
L1
100

FIG. 5

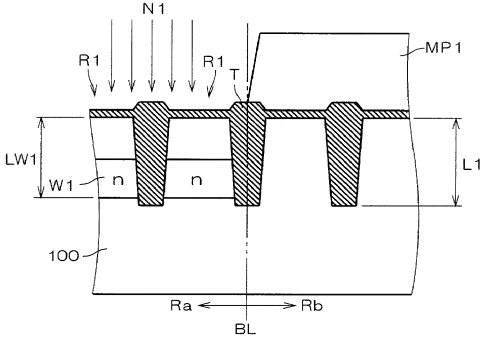

N1
R1
R1
T
MP1
LW1
W1
n
n
L1
100
Ra
Rb
BL

FIG. 6

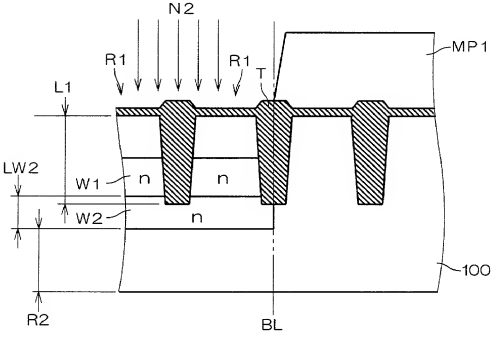

N2
R1
R1
T
MP1
L1
LW2
W1
n
n
W2
n
100
R2
BL

FIG. 7

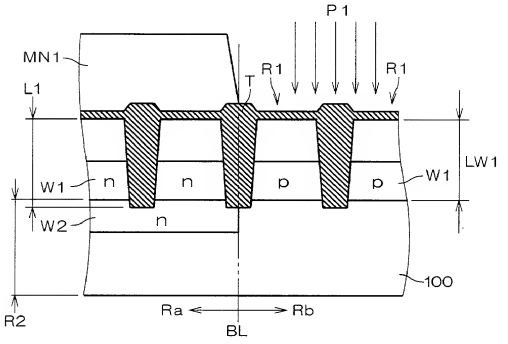

P1
MN1
L1
T
R1
R1
LW1
W1
n
n
p
p
W1
W2
n
100
R2
Ra
Rb
BL

FIG. 8

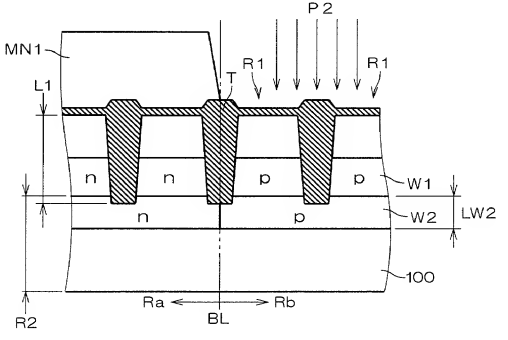

P2
MN1
L1
T
R1
R1
n
n
p
p
W1
n
p
W2
LW2
100
R2
Ra
Rb
BL

FIG. 9

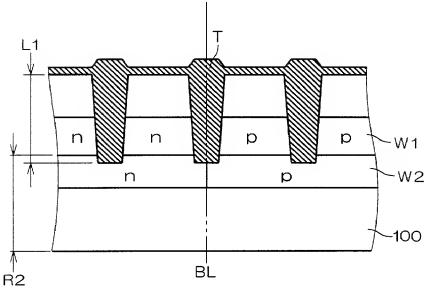

L1
T
n
n
p
p
W1
n
p
W2
100
R2
BL

FIG. 10

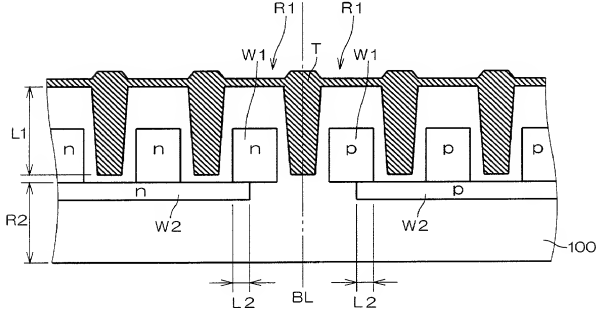

R1
R1
W1
T
W1
L1
n
n
n
p
p
p
n
p
R2
W2
W2
100
L2
BL
L2

FIG. 11

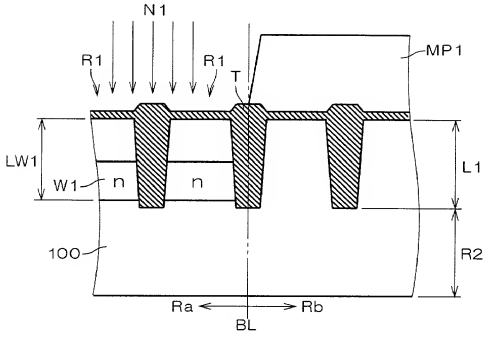

N1
R1
R1
T
MP1
LW1
W1
n
n
L1
R2
100
Ra
Rb
BL

FIG. 12

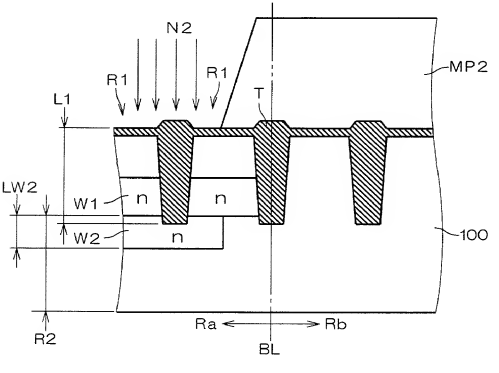

N2
R1
R1
T
MP2
L1
LW2
W1
n
n
W2
n
100
R2
Ra
Rb
BL

FIG. 13

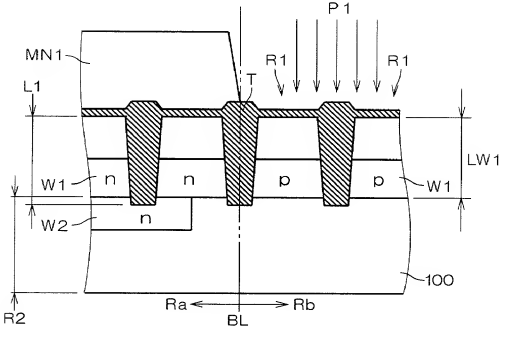

P1
MN1
R1
R1
T
L1
LW1
W1
n
n
p
p
W1
W2
n
100
R2
Ra
Rb
BL

FIG. 14

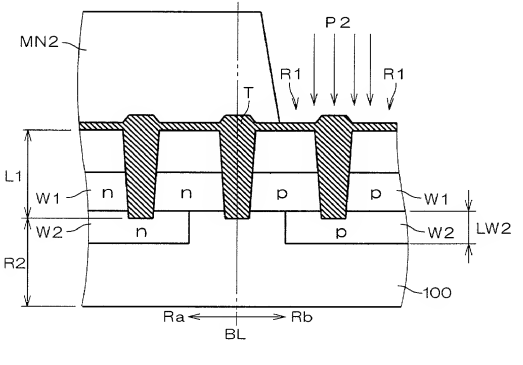

P2
MN2
R1
R1
T
L1
W1
n
n
p
p
W1
W2
n
p
W2
LW2
R2
100
Ra
Rb
BL

FIG. 15

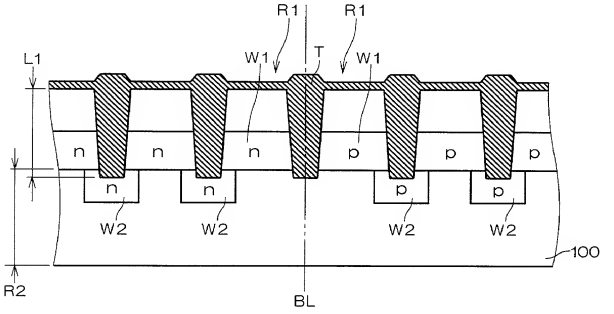

R1
R1
L1
W1
T
W1
n
n
n
p
p
p
n
n
p
p
W2
W2
W2
W2
100
R2
BL

FIG. 16

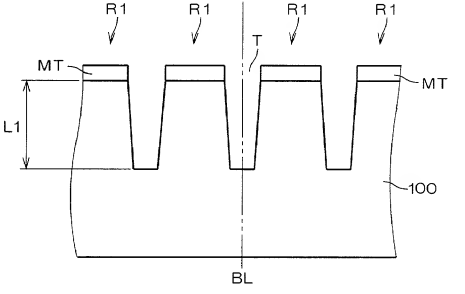

R1
R1
R1
R1
T
MT
MT
L1
100
BL

FIG. 17

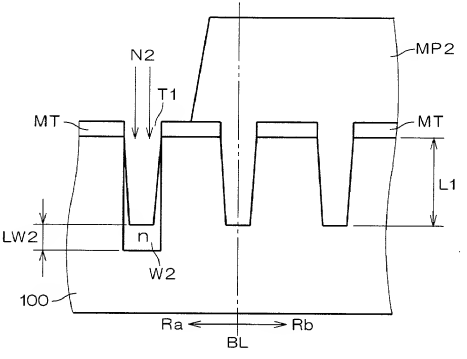

N2
T1
MP2
MT
MT
L1
LW2
n
W2
100
Ra
Rb
BL

FIG. 18

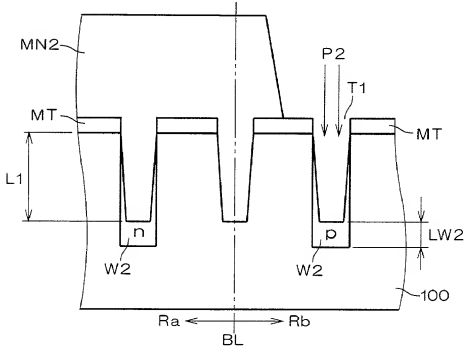

MN2
P2
T1
MT
MT
L1
n
p
LW2
W2
W2
100
Ra
Rb
BL

FIG. 19

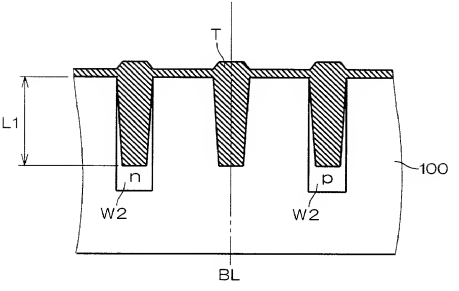


FIG. 20

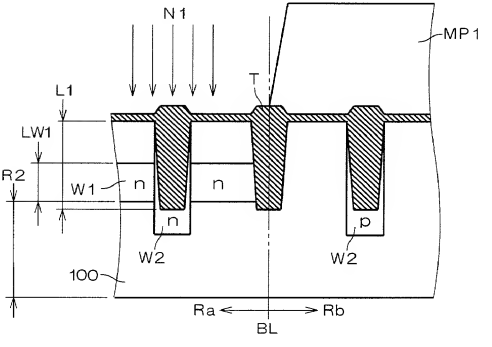


FIG. 21

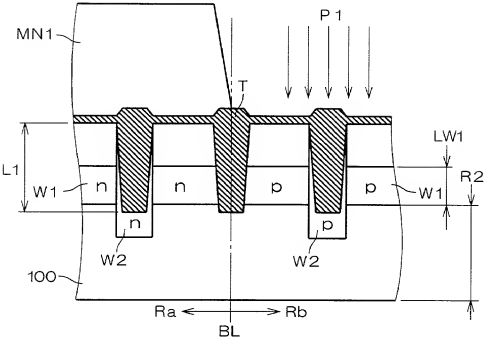

MN1
P1
T
LW1
L1
W1
n
n
p
p
W1
R2
n
p
W2
W2
100
Ra
Rb
BL

FIG. 22

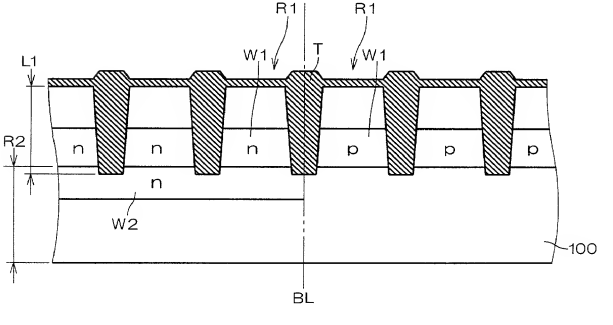

R1
R1
W1
T
W1
L1
R2
n
n
n
p
p
p
n
W2
100
BL

FIG. 23

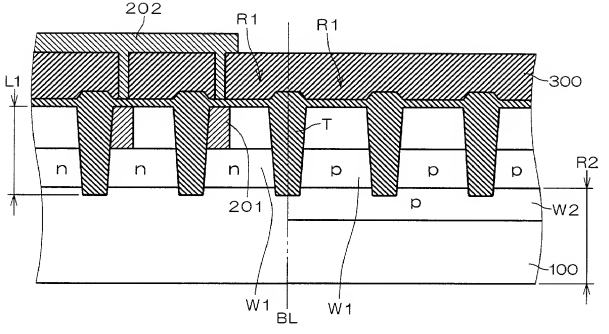

202
R1
R1
L1
300
T
n
n
n
p
p
p
R2
201
p
W2
100
W1
BL
W1

FIG. 24

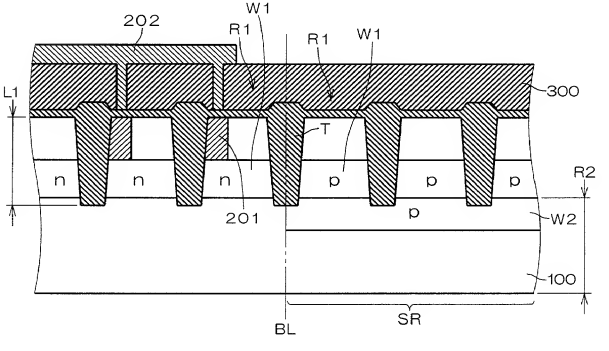

W1
202
R1
R1
W1
L1
300
T
n
n
n
p
p
p
R2
201
p
W2
100
BL
SR

FIG. 25

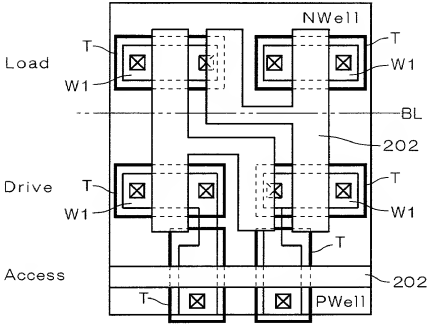

NWell
T
Load
W1
T
W1
BL
202
Drive
T
W1
T
W1
T
Access
202
T
PWell

FIG. 26

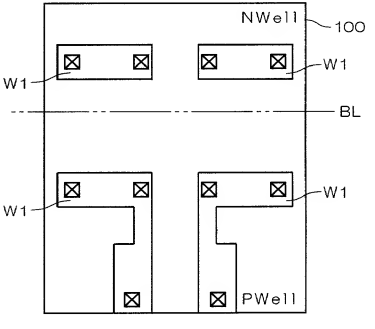

NWell
100
W1
W1
BL
W1
W1
PWell

FIG. 27

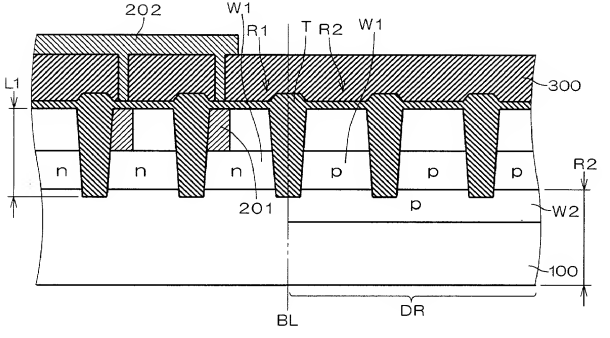

202
W1
R1
T
R2
W1
L1
300
n
n
n
p
p
p
R2
201
p
W2
100
BL
DR

FIG. 28

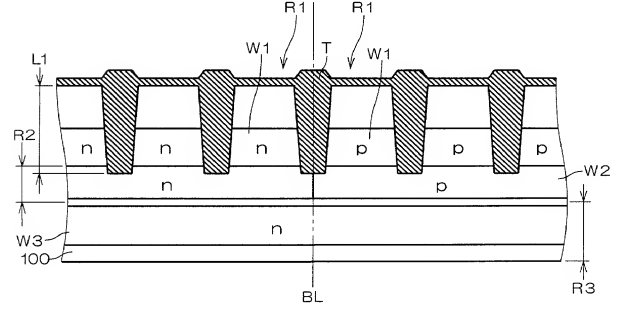

R1
R1
W1
T
W1
L1
R2
n
n
n
p
p
p
W2
n
p
n
W3
100
BL
R3

FIG. 29
< BACKGROUND ART >

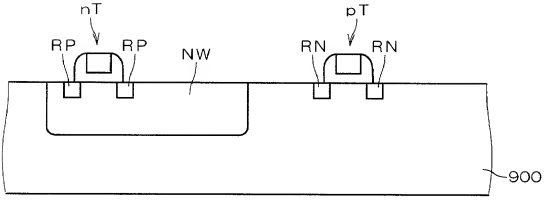


FIG. 30
< BACKGROUND ART >

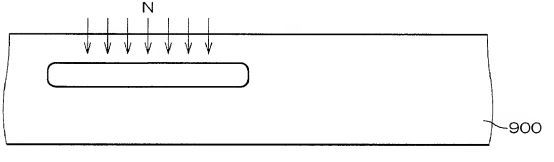


FIG. 31
< BACKGROUND ART >

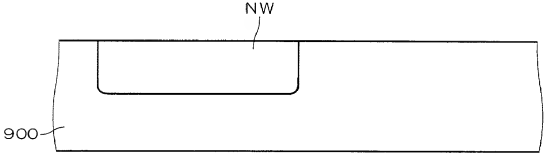


FIG. 32
< BACKGROUND ART >

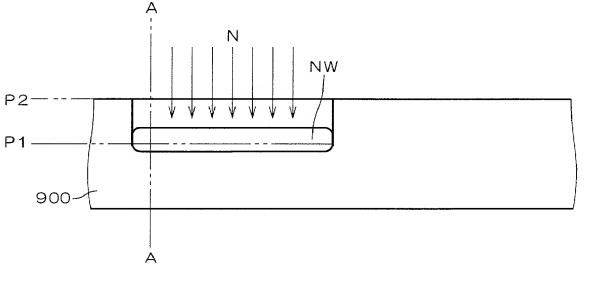


FIG. 33
< BACKGROUND ART >

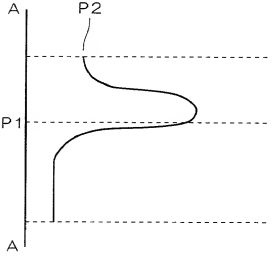


FIG. 34
< BACKGROUND ART >

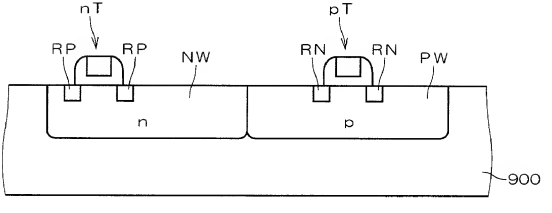


FIG. 35
< BACKGROUND ART >

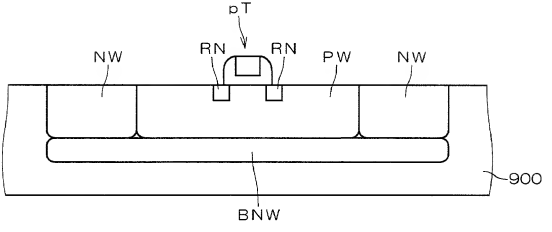


FIG. 36
< BACKGROUND ART >

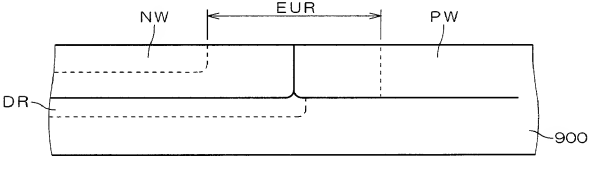


FIG. 37
< BACKGROUND ART >

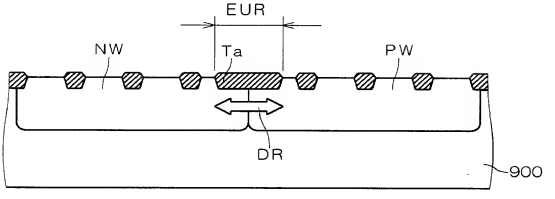


FIG. 38
< BACKGROUND ART >

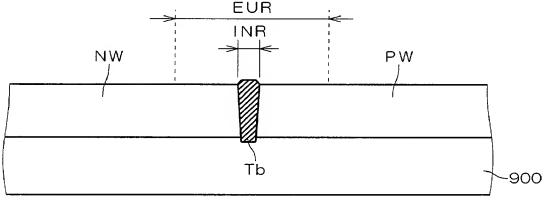


FIG. 39
< BACKGROUND ART >

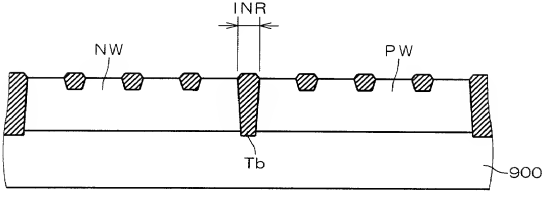


FIG. 40
< BACKGROUND ART >

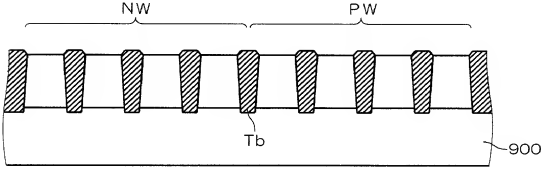


FIG. 41
< BACKGROUND ART >

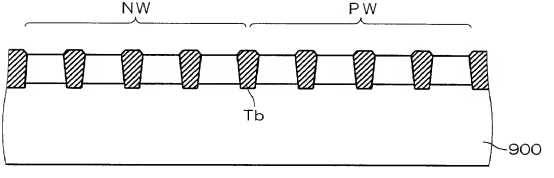


FIG. 42
< BACKGROUND ART >

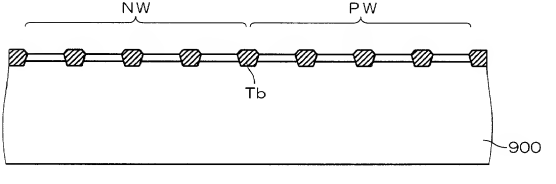


FIG. 43
< BACKGROUND ART >

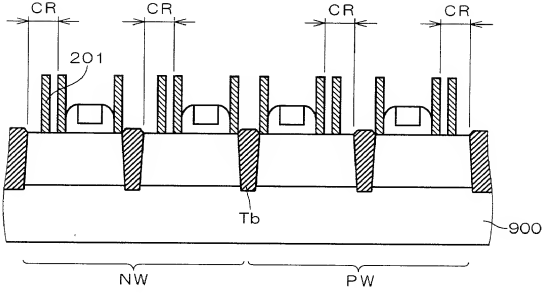


FIG. 44
< BACKGROUND ART >

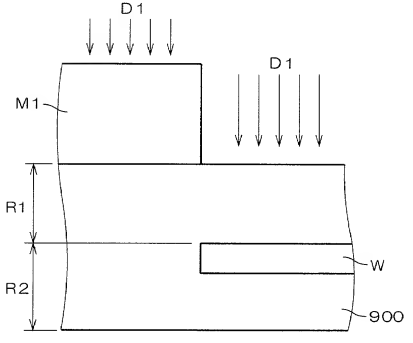
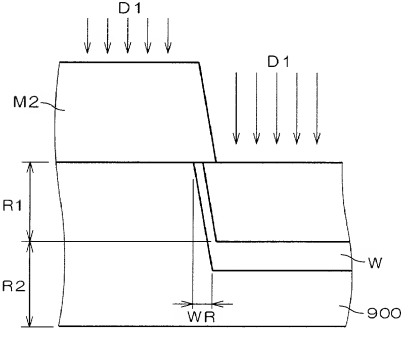


FIG. 45
< BACKGROUND ART >



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF

上記発明の明細書は、

☐ 本書に添付されています。

☐ ___月___日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
（該当する場合）_____に訂正されました。

the specification of which

☒ is attached hereto.

☐ was filed on _____
as United States Application Number or
PCT International Application Number
_____ and was amended on
_____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条（a）-（d）項又は365条（b）項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365（a）項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Claimed 優先権主張 Yes はい	No いいえ
P11-97417	JAPAN	April 5, 1999	☒	☐
			☐	☐

私は、第35編米国法典119条（e）項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条（c）に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
(弁護士、または代理人の指名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

Norman F. Oblon, Registration Number 24,618; Marvin J. Spivak, Registration Number 24,913; C. Irvin McClelland, Registration Number 21,124; Gregory J. Maier, Registration Number 25,599; Arthur I. Neustadt, Registration Number 24,854; Richard D. Kelly, Registration Number 27,757; James D. Hamilton, Registration Number 28,421; Eckhard H. Kuesters, Registration Number 28,870; Robert T. Pous, Registration Number 29,099; Charles L. Gholz, Registration Number 26,395; Vincent J. Sunderdick, Registration Number 29,004; William E. Beaumont, Registration Number 30,996; Steven B. Kelber, Registration Number 30,073; Robert F. Gnuse, Registration Number 27,295; Jean-Paul Lavalleye, Registration Number 31,451; Stephen G. Baxter, Registration Number 32,884; Martin M. Zoltick, Registration Number 35,745; Robert W. Hahl, Registration Number 33,893; Richard L. Treanor, Registration Number 36,379; Steven P. Weihrouch, Registration Number 32,829; John T. Goolkasian, Registration Number 26,142; Marc R. Labgold, Registration Number 34,651; William J. Healey, Registration Number 36,160; Richard L. Chinn, Registration Number 34,305; Steven E. Lipman, Registration Number 30,011; Carl E. Schiller, Registration Number 34,426; James J. Kulbaski, Registration Number 34,648; Catherine B. Richardson, Registration Number 39,007; Richard A. Neifeld, Registration Number 35,299; and J. Derek Mason, Registration Number 35,270; with full powers of substitution and revocation.

書類送付先

Send Correspondence to:

OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C.
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VIRGINIA 22202 U.S.A.

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)
(703) 413-3000

唯一または第一発明者名	Full name of sole or first inventor Shuuichi UENO
発明者の署名　日付	Inventor's signature　Date Shuuichi Ueno　August 18, 1999
住所	Residence　TOKYO, JAPAN
国籍	Citizenship　JAPAN
私書箱	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha, 2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN
第二共同発明者	Full name of second joint inventor, if any Tomohiro YAMASHITA
第二共同発明者の署名　日付	Second Inventor's signature　Date Tomohiro Yamashita　August 18, 1999
住所	Residence　TOKYO, JAPAN
国籍	Citizenship　JAPAN
私書箱	Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha, 2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

(第三以降の共同発明者についても同様に記載し、署名すること)

(Supply similar information and signature for third and subsequent joint inventors.)

Japanese Language Declaration
（日本語宣言書）

第三の共同発明者の氏名		Full name of third joint inventor, if any Hidekazu ODA
第三の共同発明者の署名	日付	Third joint Inventor's signature Hidekazu Oda Date August 18, 1999
住所		Residence TOKYO, JAPAN
国籍		Citizenship JAPAN
郵便の宛先		Post Office Address c/o Mitsubishi Denki Kabushiki Kaisha, 2-3, Marunouchi 2-chome, Chiyoda-ku, TOKYO 100-8310 JAPAN

第四の共同発明者の氏名		Full name of fourth joint inventor, if any
第四の共同発明者の署名	日付	Fourth joint Inventor's signature Date
住所		Residence
国籍		Citizenship
郵便の宛先		Post Office Address

第五の共同発明者の氏名		Full name of fifth joint inventor, if any
第五の共同発明者の署名	日付	Fifth joint Inventor's signature Date
住所		Residence
国籍		Citizenship
郵便の宛先		Post Office Address

第六の共同発明者の氏名		Full name of sixth joint inventor, if any
第六の共同発明者の署名	日付	Sixth joint Inventor's signature Date
住所		Residence
国籍		Citizenship
郵便の宛先		Post Office Address